FIG.1

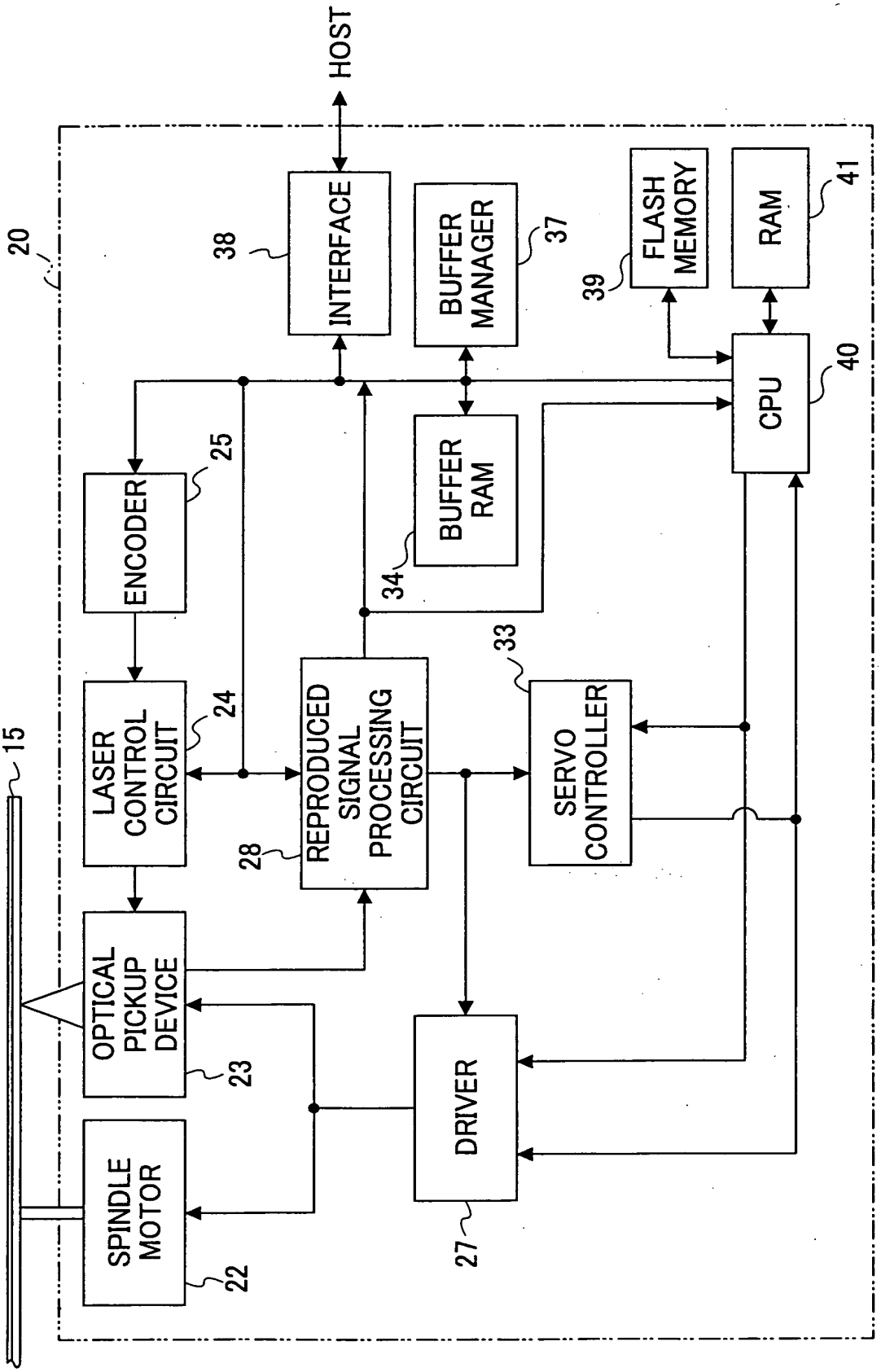
HOST
20
38
INTERFACE
BUFFER MANAGER
37
39
FLASH MEMORY
RAM
41
CPU
40
BUFFER RAM
34
25
ENCODER
33
LASER CONTROL CIRCUIT
24
REPRODUCED SIGNAL PROCESSING CIRCUIT
28
SERVO CONTROLLER
15
OPTICAL PICKUP DEVICE
23
DRIVER
27
SPINDLE MOTOR
22

FIG.2

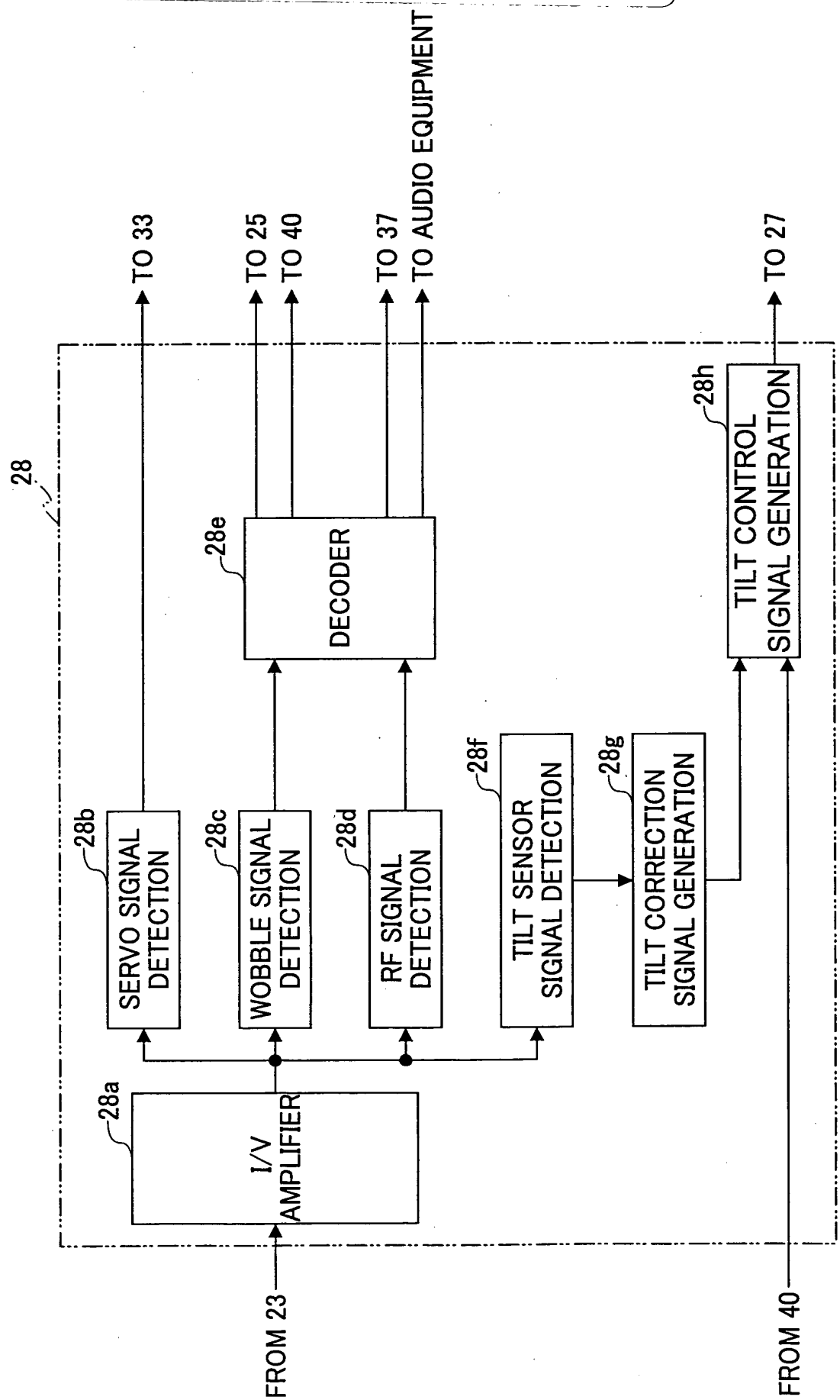
28
TO 33
TO 25
TO 40
TO 37
TO AUDIO EQUIPMENT
TO 27
28e
DECODER
28h
TILT CONTROL SIGNAL GENERATION
28b
SERVO SIGNAL DETECTION
28c
WOBBLE SIGNAL DETECTION
28d
RF SIGNAL DETECTION
28f
TILT SENSOR SIGNAL DETECTION
28g
TILT CORRECTION SIGNAL GENERATION
28a
I/V AMPLIFIER
FROM 23
FROM 40

FIG.3

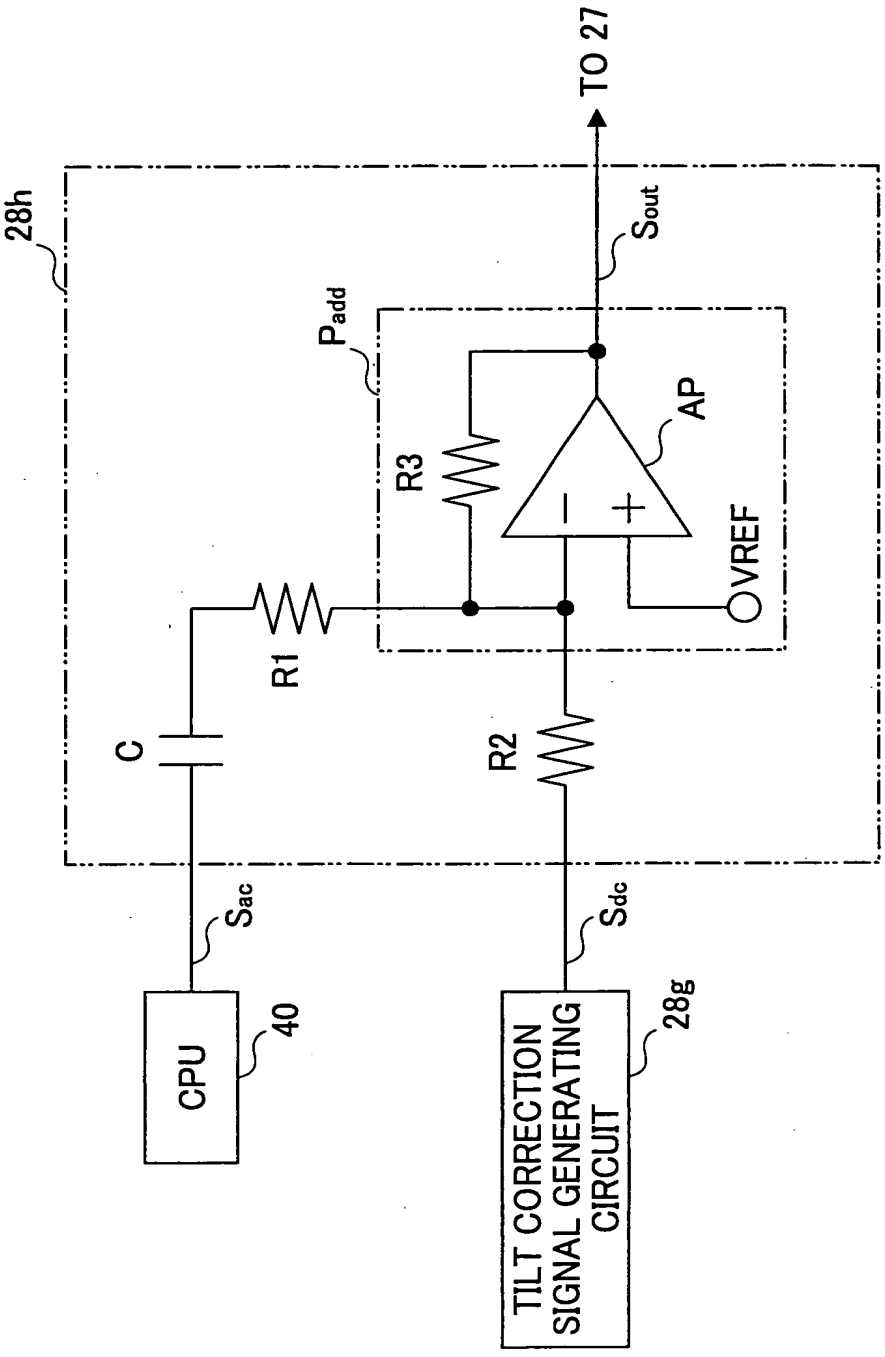
TO 27
28h
Sout
Padd
AP
R3
VREF
R1
C
R2
Sac
Sdc
CPU
40
TILT CORRECTION SIGNAL GENERATING CIRCUIT
28g

FIG.4

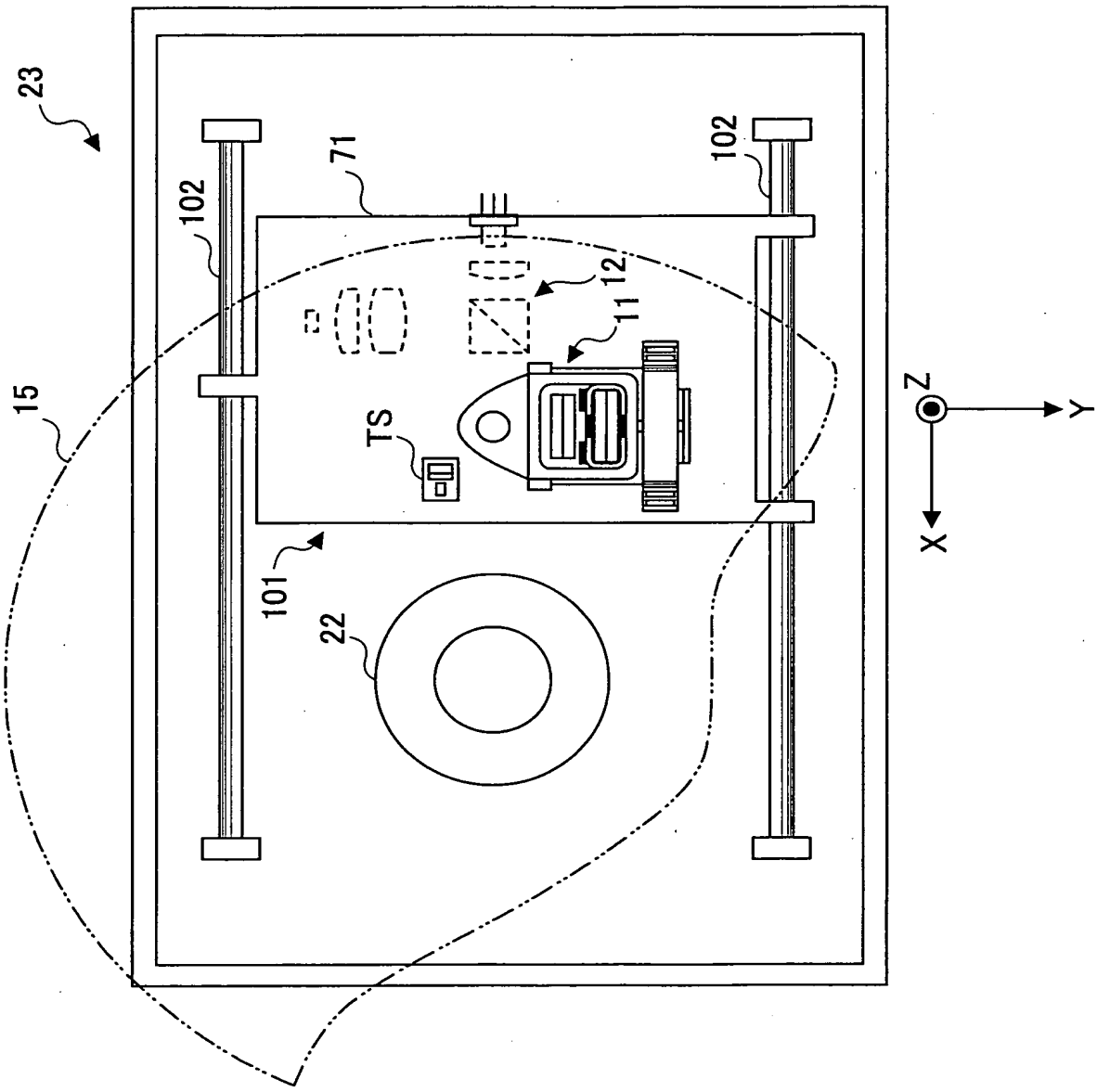

FIG.5

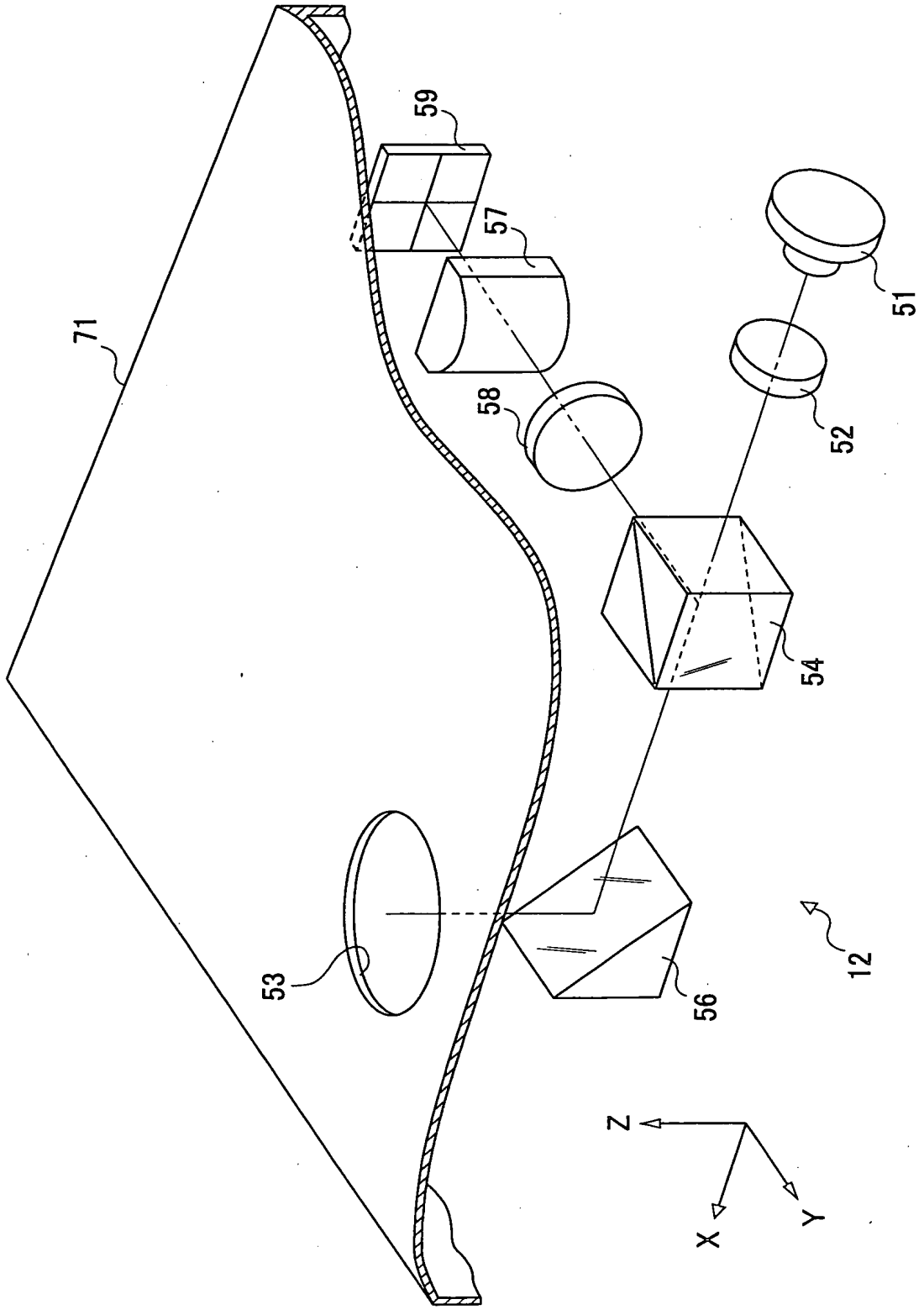

FIG.6A

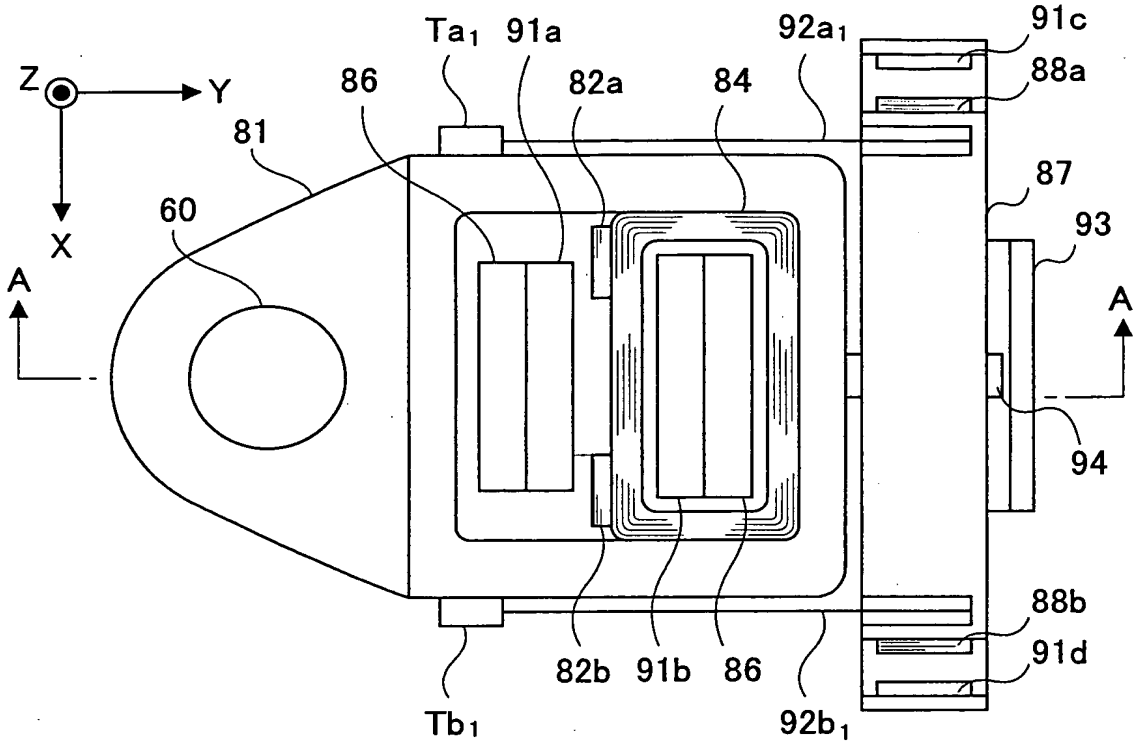
Z
Y
X
A
A
81
60
86
Ta1
91a
82a
84
92a1
91c
88a
87
93
94
88b
91d
82b
91b
86
92b1
Tb1

FIG.6B

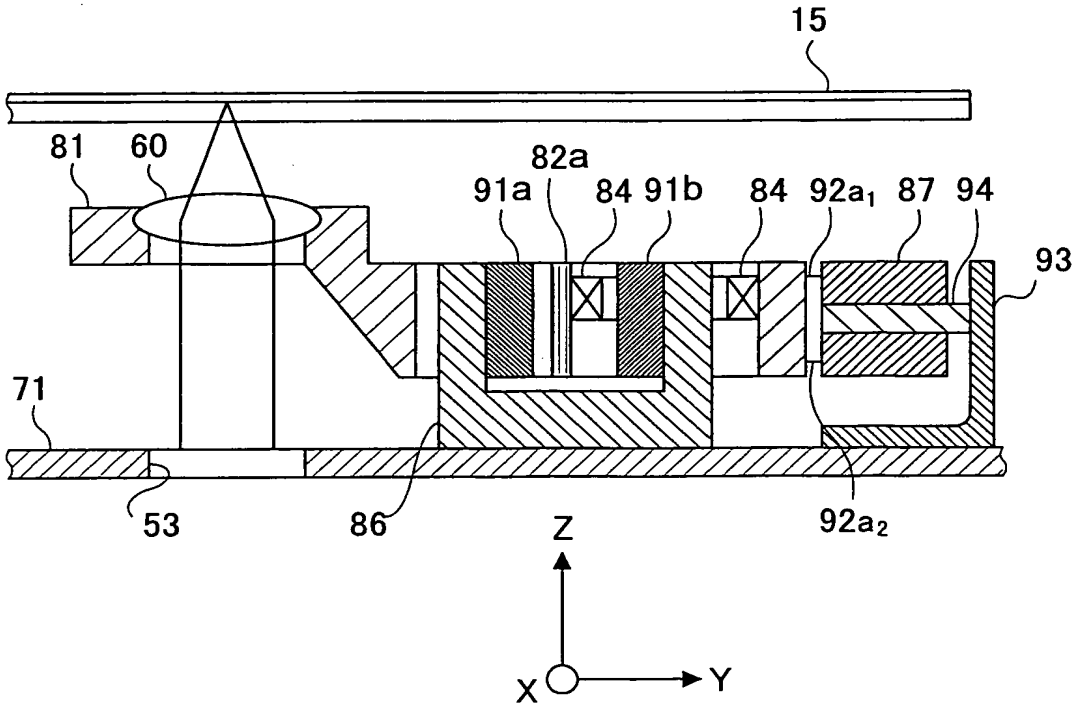
15
81
60
82a
91a
84
91b
84
92a1
87
94
93
71
53
86
92a2
Z
X
Y

FIG.7A

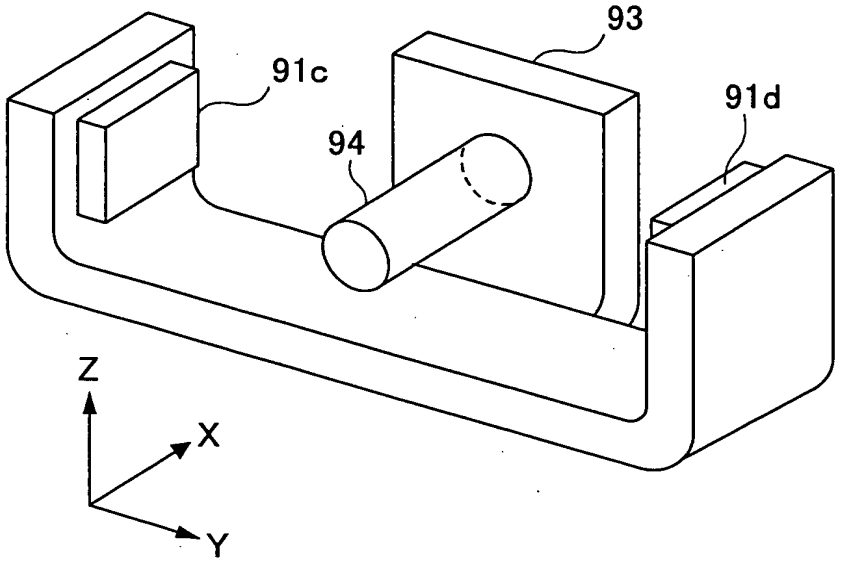

FIG.7B

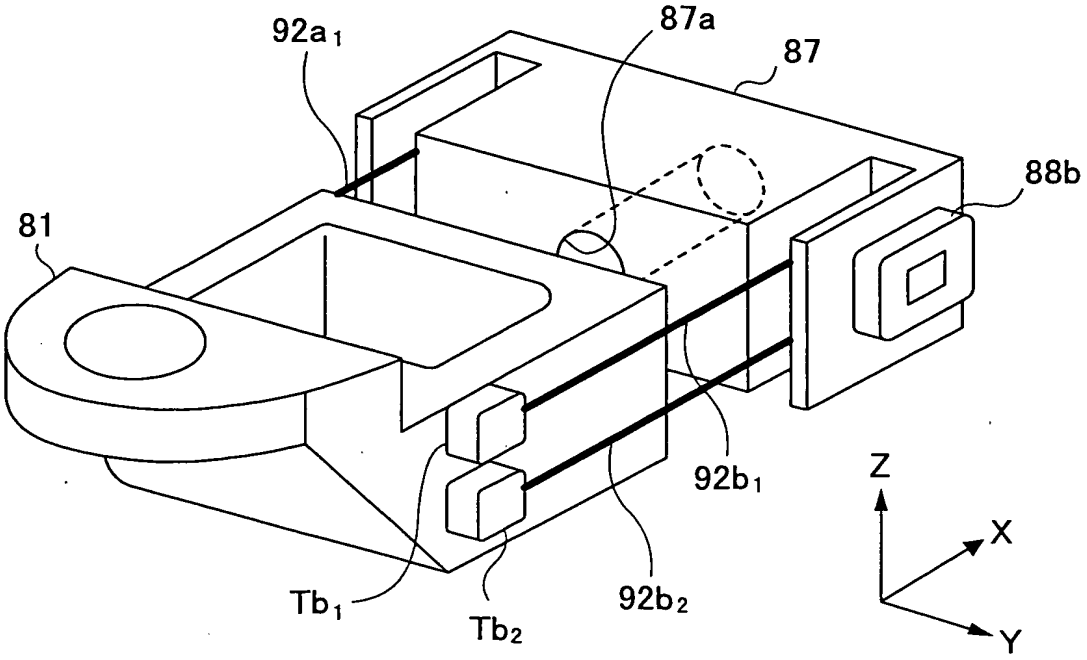

FIG.8A

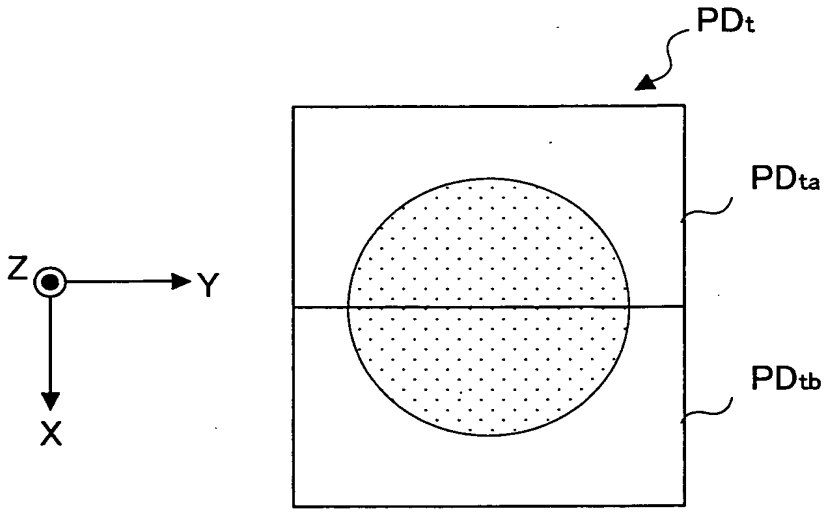

FIG.8B

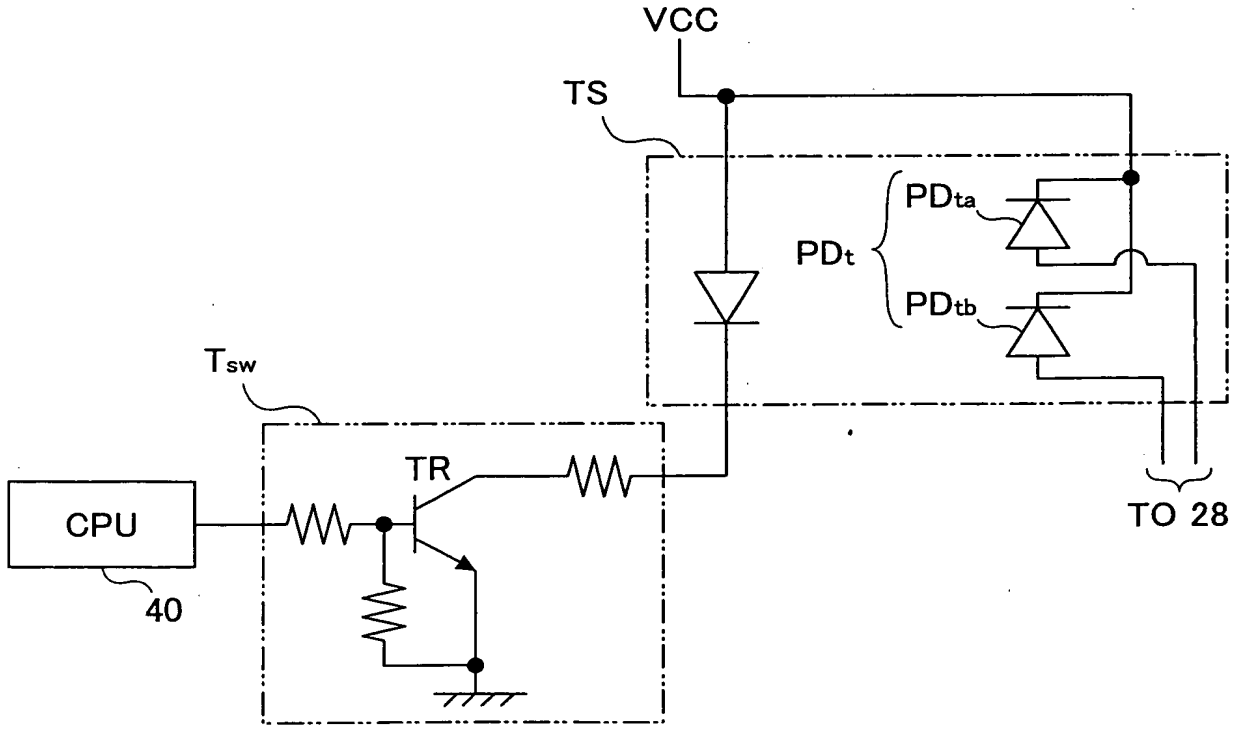

FIG.9

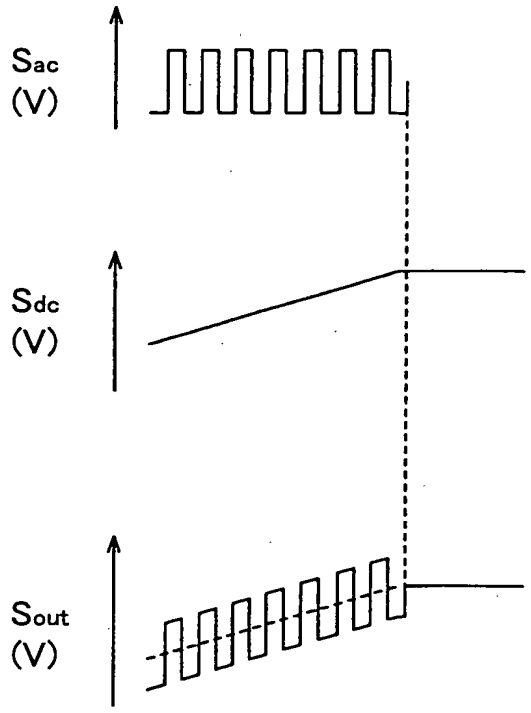

FIG.10A

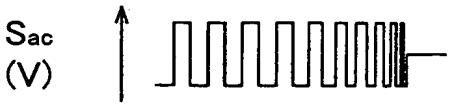

FIG.10B

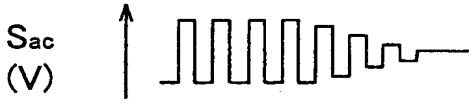

FIG.10C
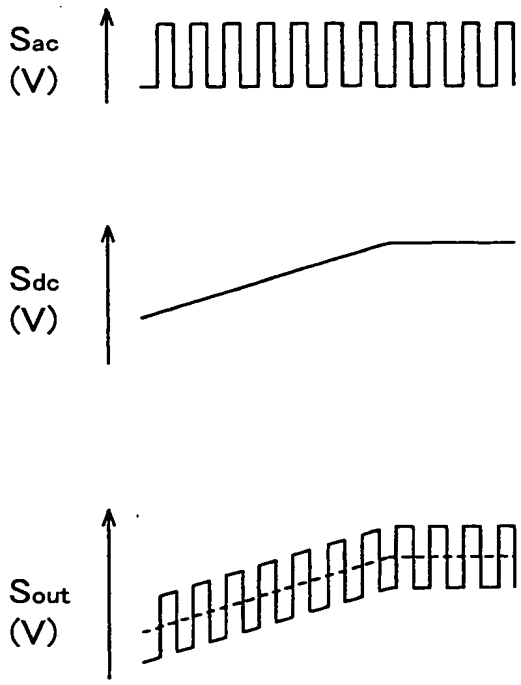
FIG.11